CLAIMS

What is claimed is:

1. A method for providing an interconnect on a semiconductor device comprising the steps of:

(a) providing a semiconductor substrate with a plurality of device structures thereon;

(b) providing at least one slot in the semiconductor substrate, and

(c) providing a metal within the at least one slot.

2. The method of claim 1 wherein the semiconductor substrate providing step (a) further comprises:

(a1) providing a substrate region;

(a2) providing an epitaxial (EPI) layer over the substrate region; and

(a3) etching a plurality of device structures in the EPI layer.

3. The method of claim 1 wherein the at least one slot providing step (b) includes the step of (b1) oxidizing the at least one slot.

4. The method of claim 2 wherein the at least one slot providing (b) comprises (b1) providing the slot to the surface of the EPI layer.

5. The method of claim 1 wherein the at least one metal providing step (c)

comprises the step of:

(c1) filling the slot utilizing a metal that is provided on the surface of the EPI layer that is of a thickness that is one-half the depth or width of the at least one slot.

6. The method of claim 1 wherein the at least one metal comprises a plurality of metals.

7. The method of claim 6 wherein the plurality of metals comprises two metals, a first metal covers one half the slot depth and a second metal fills the slot.

8. The method of claim 6 wherein the plurality of metals comprises three metals, wherein the first and second metal fill the slot and the third metal provides an interconnect layer.

9. The method of claim 3 wherein the oxide is removed from the bottom of the slot and the interconnect forms a low resistance to ground.

10. The method of claim 3 wherein a buried layer is under the slot, the oxide is removed from the bottom of the slot, and the interconnect forms a low resistance sinker.

11. The method of claim 1 wherein the at least one metal is provided utilizing chemical vapor deposition.

12. The method of claim 1 wherein the at least one metal is provided utilizing maskless sputter depositions.

13. The method of claim 12 wherein the slot edges are shaped via oxidation.

14. The method of claim 13 wherein the slot edges are shaped via depositing a photoresist on the metal and planar etching the photoresist, the metal in the field, a slight oxide etch , and then removal of the resist.

15. The method of claim 14 wherein spin on glass is utilized for the planar etching.

16. A semiconductor device comprising:

a semiconductor substrate, the semiconductor substrate including a plurality of device structures thereon; and

an interconnect on the semiconductor substrate, the interconnect comprising at least one slot provided in the semiconductor substrate and at least one metal within the slot.

17. The semiconductor device of claim 16 wherein the semiconductor substrate comprises:

a substrate region; and a buried layer, or Boron Up Diffusion where required and

an epitaxial (EPI) layer over the substrate region, wherein the device structures are provided in the EPI layer.

18. The semiconductor device of claim 17 wherein the at least one metal comprises a plurality of metals.

19. The semiconductor device of claim 18 wherein the plurality of metals comprises two metals, a first metal covers one-half of the slot and a second metal fills the slot.

20. The semiconductor device of claim 19 wherein the plurality of metals comprises three metal depositions, wherein the first and second deposition of metal fill the slot and a third metal deposition provides the interconnect layer.

21. The semiconductor device of claim 16 wherein the at least one metal is provided utilizing chemical vapor deposition.

22. The semiconductor device of claim 16 wherein the at least one metal is provided utilizing sputter depositions.

23. A high current, high power interconnect on a semiconductor substrate comprising:

at least one slot provided in the semiconductor substrate; and

at least one metal within the slot.

24. The high current, high power interconnect of claim 23 wherein the semiconductor substrate comprises:

a substrate region; and

an epitaxial (EPI) layer over the substrate region, wherein the device structures are provided in the EPI layer.

25. The high current interconnect of claim 24 with at least one metal comprises a plurality of metals.

26. The high current interconnect of claim 25 wherein the plurality of metals comprises two metals, a first meal covers one-half of the slot and a second metal fills the slot.

27. The high current interconnect of claim 25 wherein the plurality of metals comprises three metals, wherein the first and second metal fill the slot and the third metal provides an interconnect layer.

28. The high current interconnect of claim 23 wherein the at least one metal is provided utilizing chemical vapor deposition.

29. The high current interconnect of claim 23 wherein the at least one metal is provided utilizing sputter deposition.